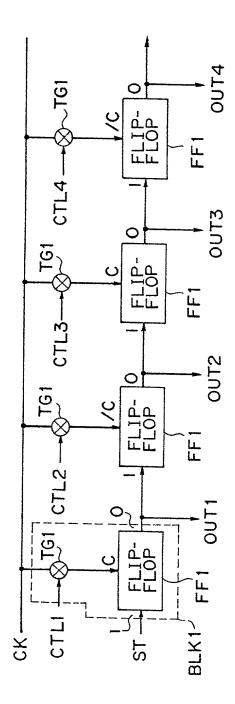
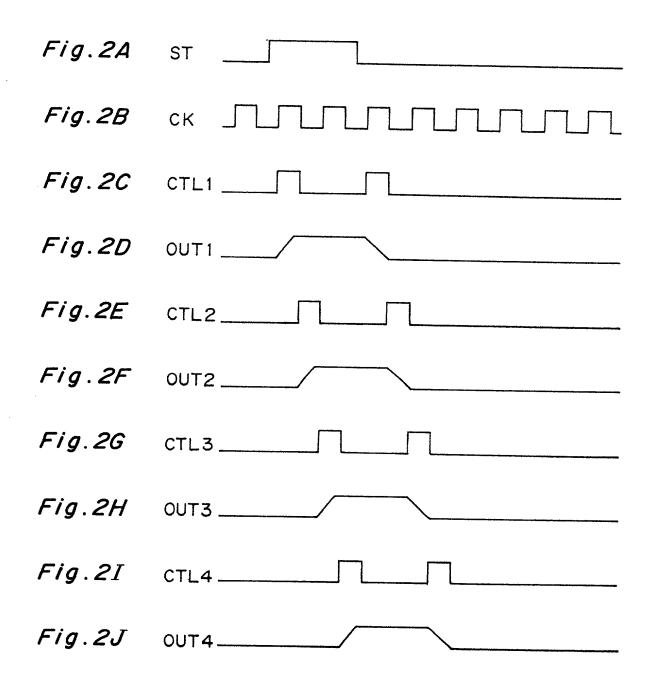
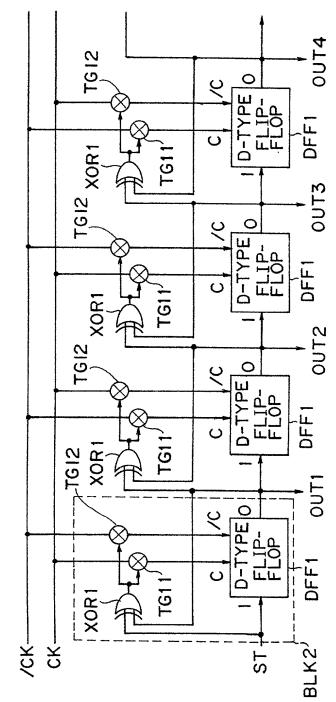
Fig. 1

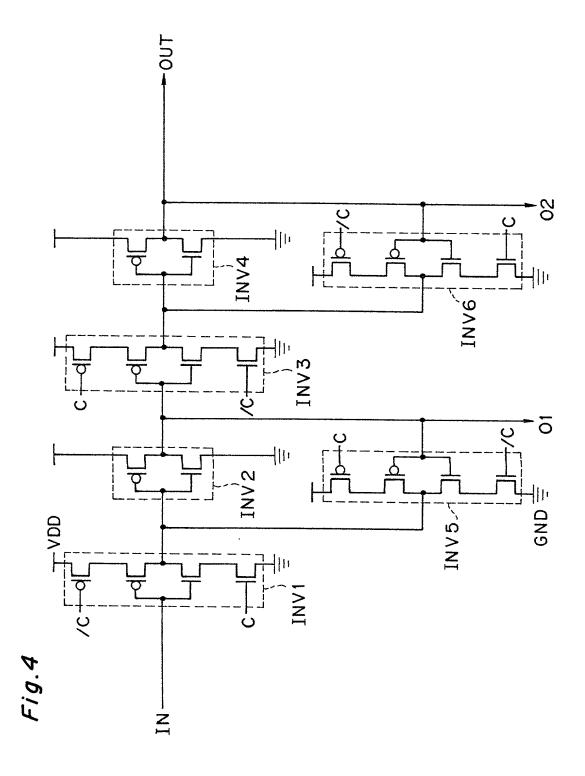
....

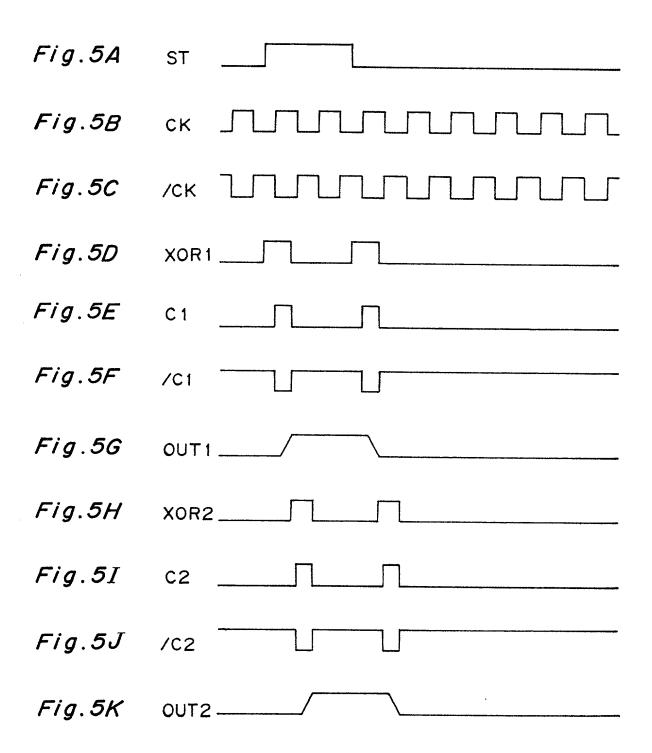




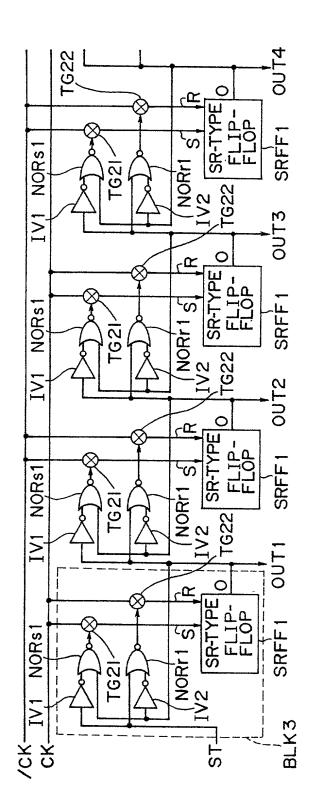








F19.6



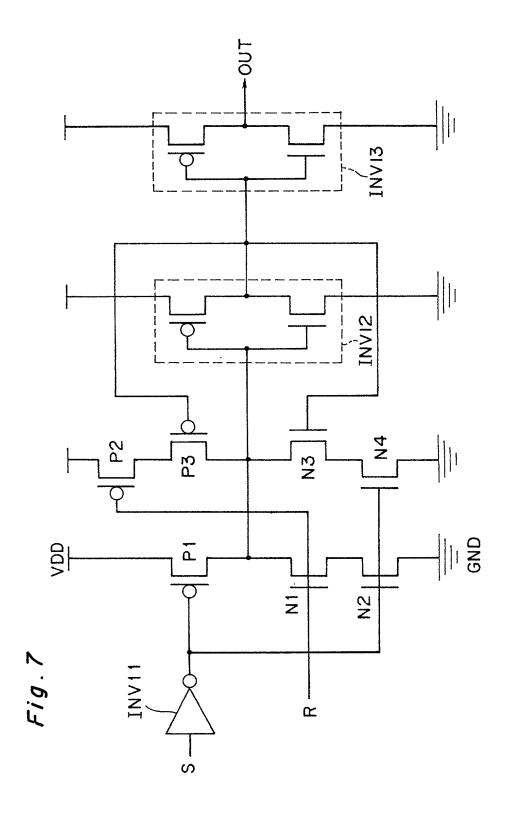
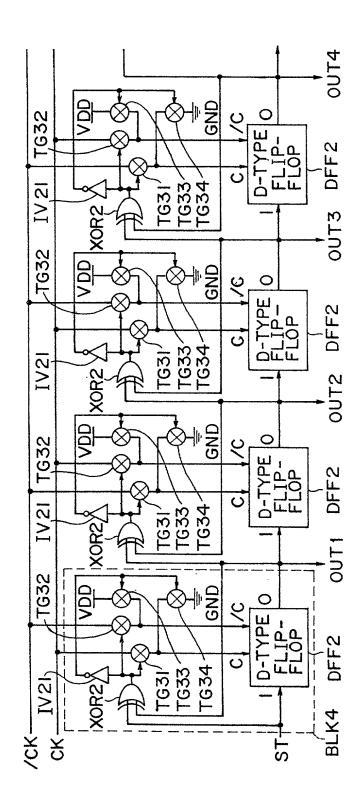
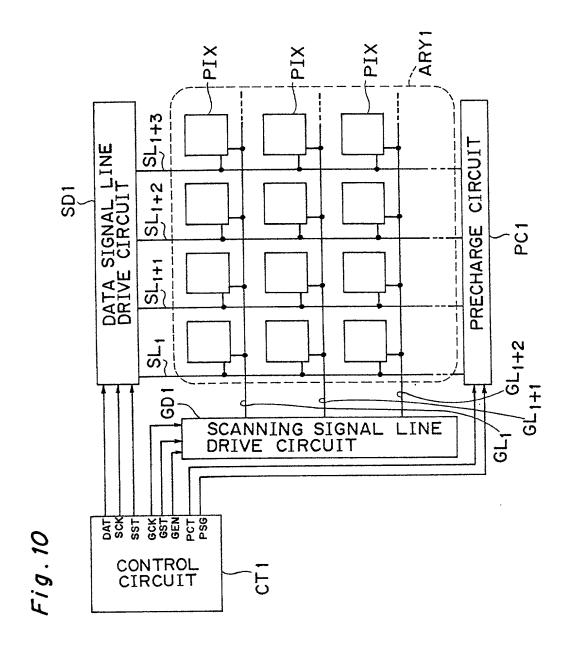


Fig.8A	ST
Fig.8B	ск
Fig.8C	/ck
Fig.8D	NORs1
Fig.8E	NORr1
Fig.8F	S1
Fig.8G	R1
Fig.8H	OUT1
Fig.8I	NORs2
Fig.8J	NORr2
Fig.8K	s2
Fig.8L	R2
Fig.8M	OUT2

Fig. 9





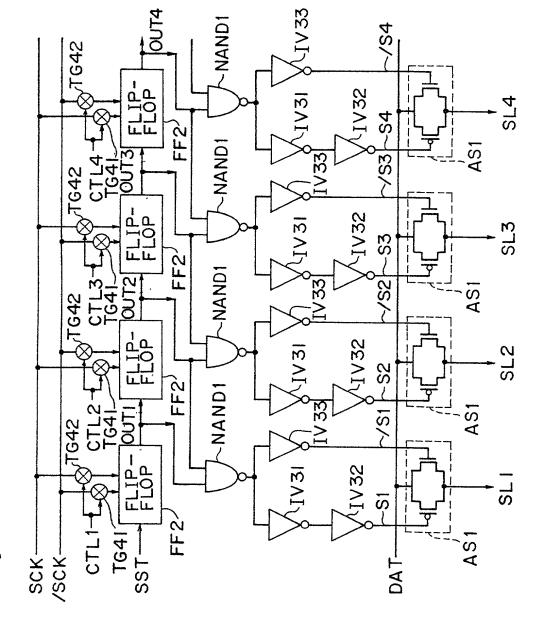
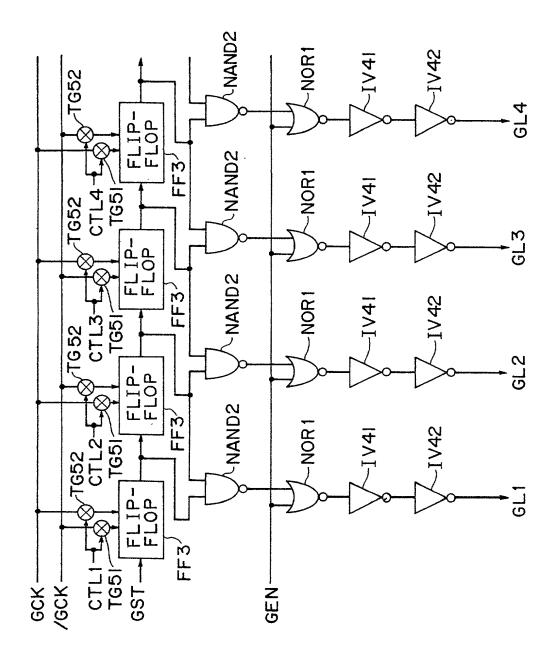
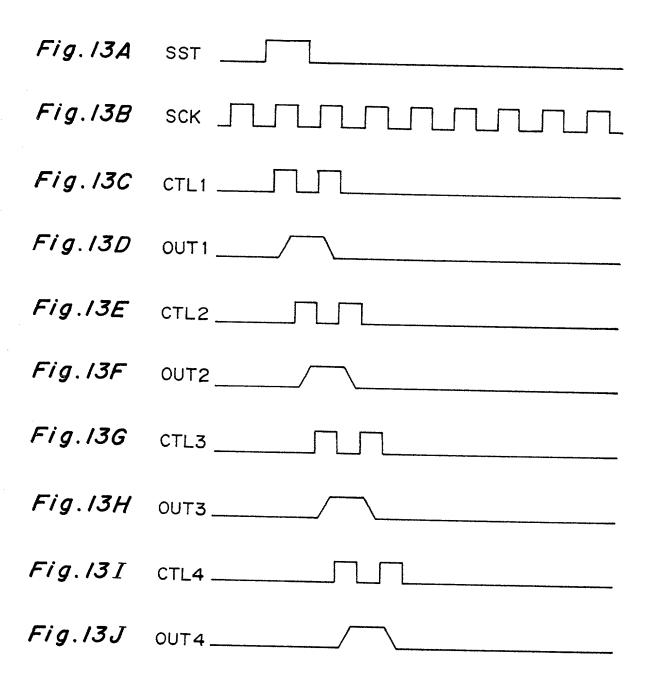


Fig. 11

Fig. 12





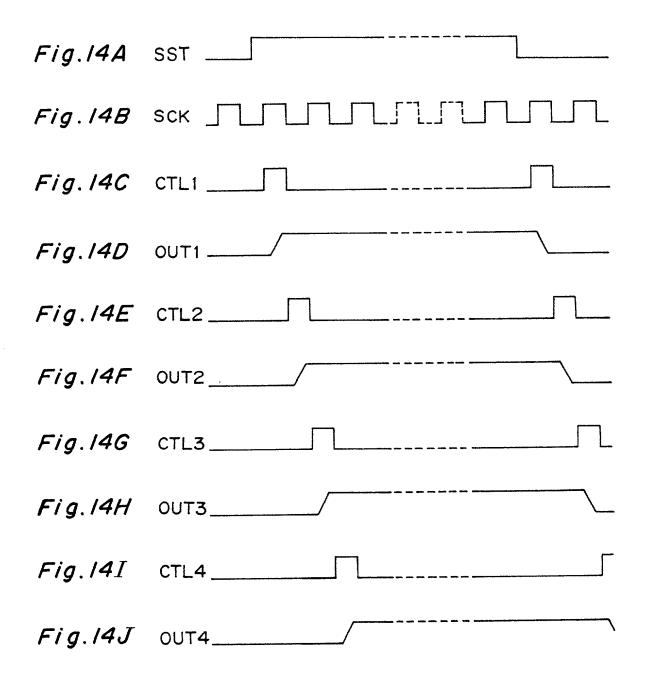
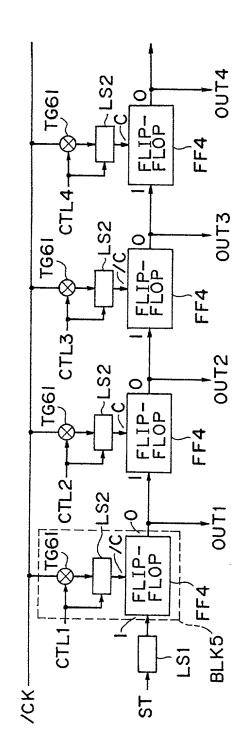


Fig. 15



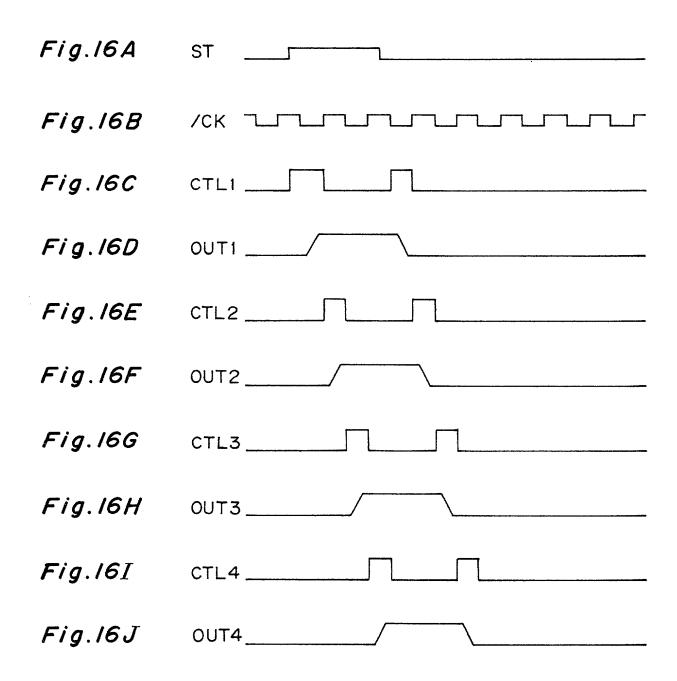
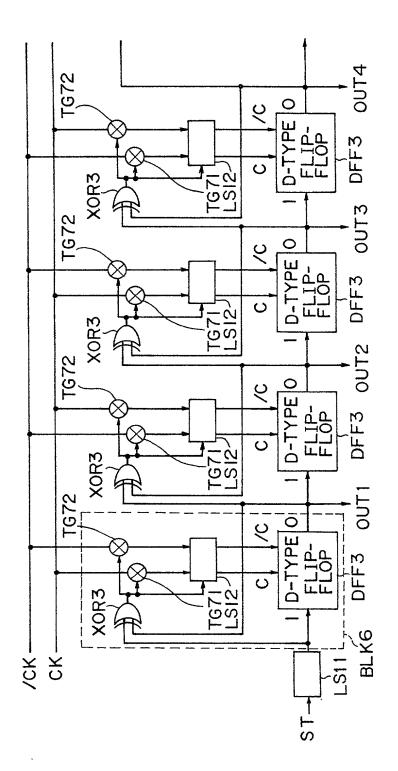


Fig.17



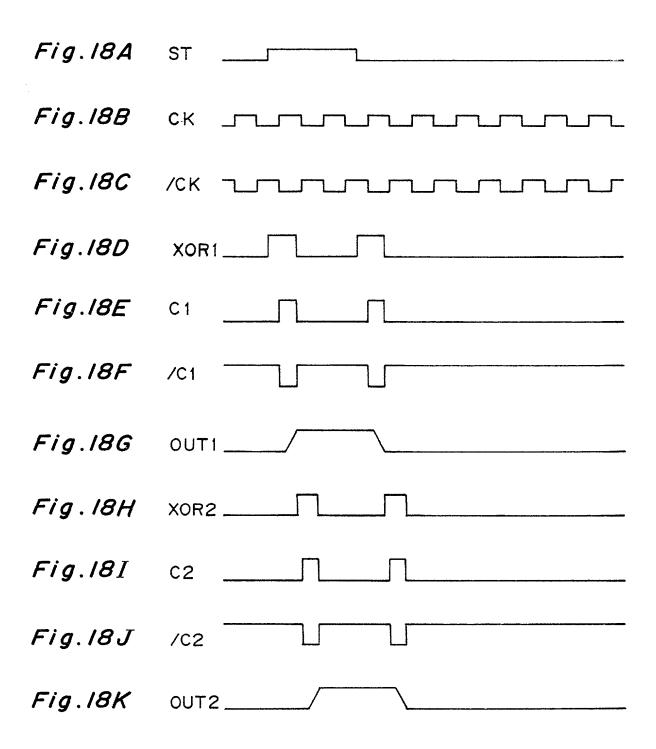
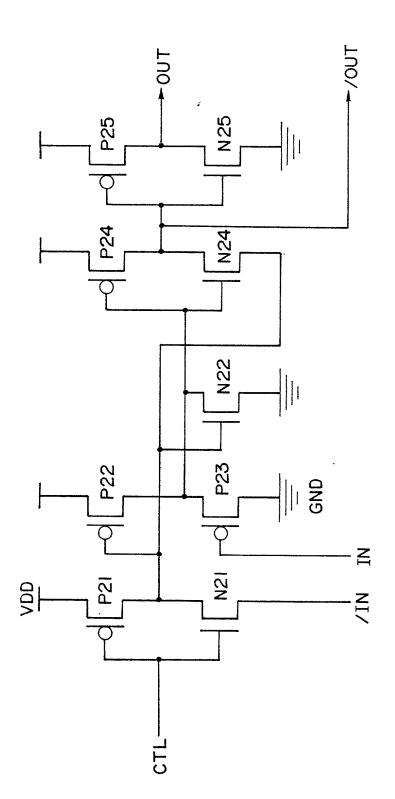
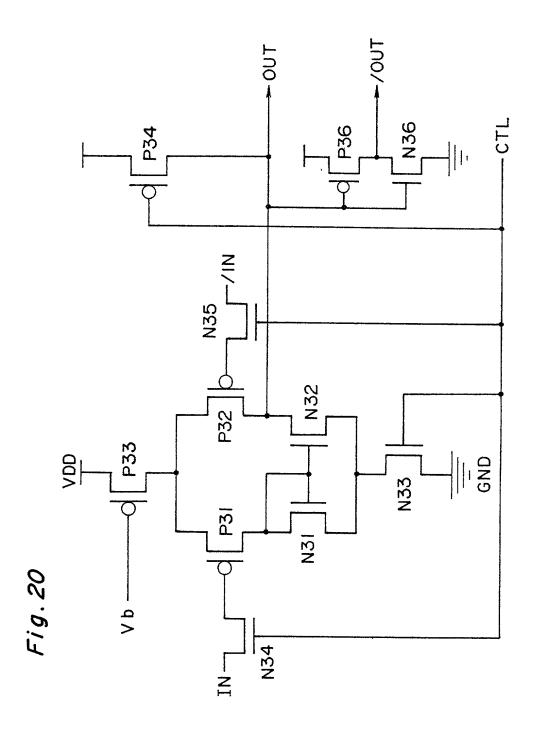


Fig. 19





SR-TYPE FLIP-SRFF2 NOR'r2 NOR_{\$}2 **TG8**1 IV 52 -TG82 LS22 **IV** 51 **OUT3** 0 SR-TYPE FLIP-FLOP Œ, SRFF2 NORr2 S NORs2 TG81-IV52 -T682 LS22 1051 OUT2 0 S R SR-TYPE SRFF2 NORs2 IV 52 TG82 LS22 **T**681 18/1 OUT1 SR-TYPE OF FLIP-SRFF2 S NORs2 NOR'2 TG81-Fig. 21 IV 52 LS22-1751 /CKI LS2I ST+

0

S

TG82

Fig. 22 A	ST
Fig.22B	CK Trintri
Fig.22C	/CK ~_~_~_~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Fig.22D	NORs1
Fig.22E	NORr1
Fig.22F	S1
Fig.22G	R1
Fig.22H	OUT1
Fig.22I	NORs2
Fig.22J	NORr2
Fig.22K	s2
Fig. 22L	R2
Fia.22M	OUT2

and the second of the second o

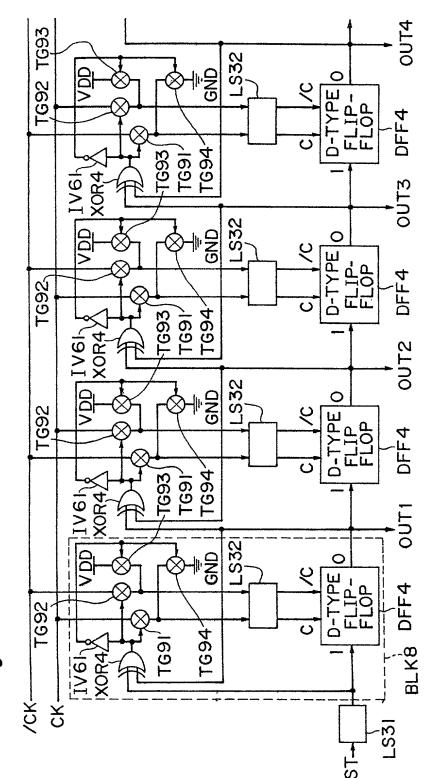
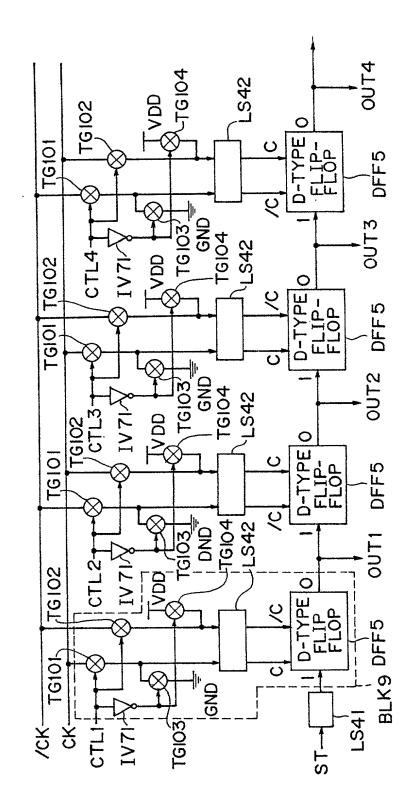


Fig.23

Fig. 24



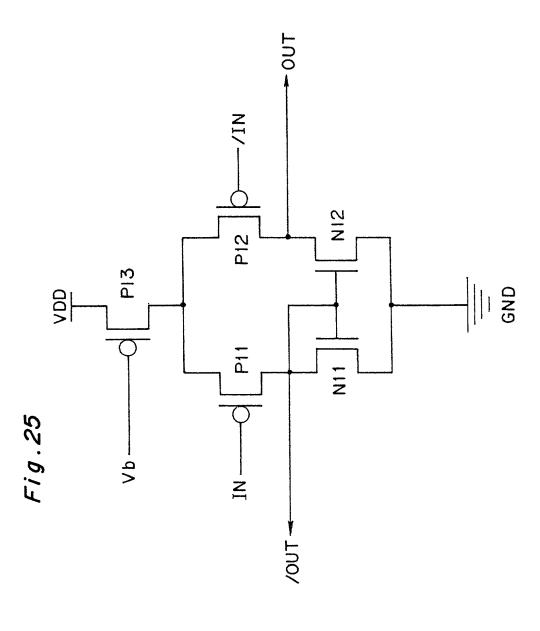
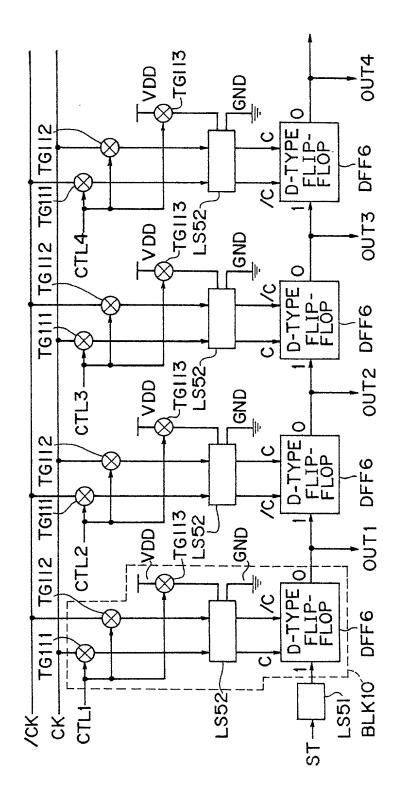


Fig. 26

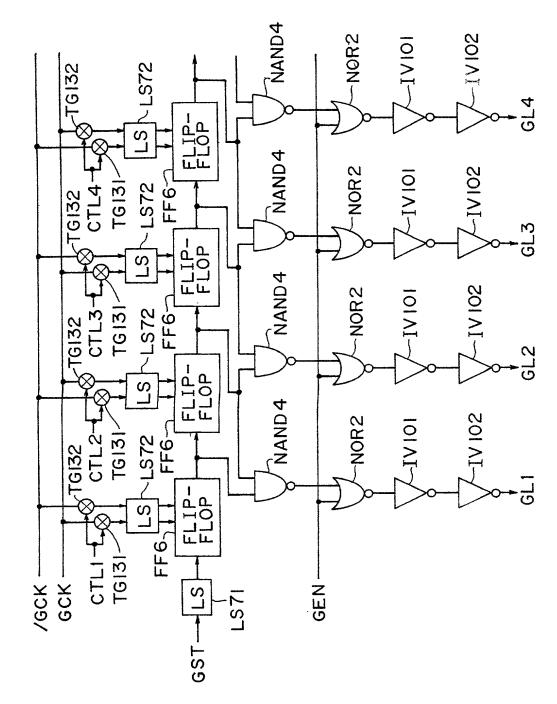


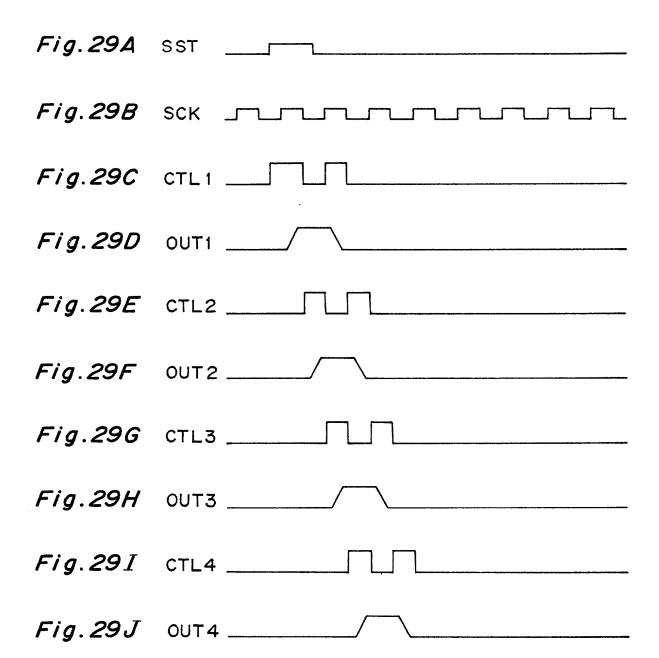
TG122

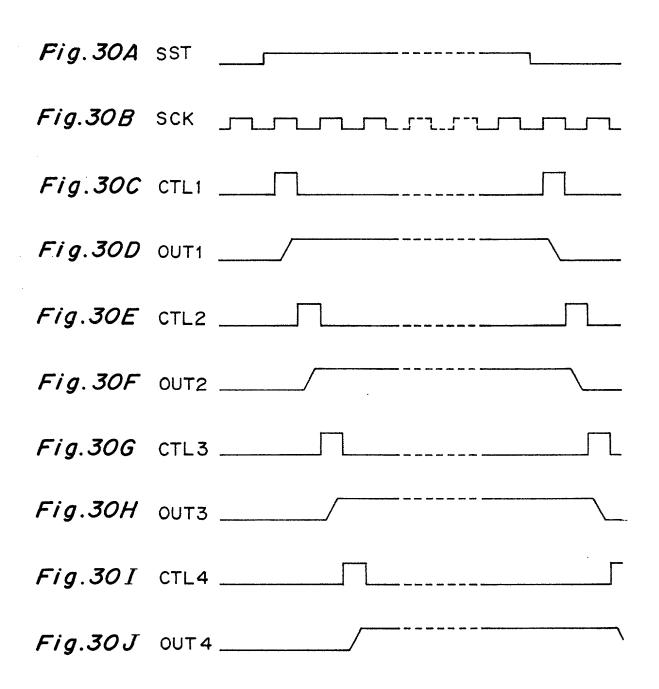
(~IV92 \I\V9I **SL4** -S4 FF5 **NAND3** AS2 [V93] LS62 0UT3 -/53 TG121 TG122 _IV92 FLIT SL3 -83 FF5 **NAND3** ~LS62 0UT2 /82 **TG12**F **G122** LIP-.IV92 -\$2 FF5² **NAND3** AS2 TG121/ IS/ **TG122** FLIP-FLOP \IN92 SL1 S FF5 Fig. 27 TG121-/SCK | AS2 LS6I SST-

\\-\NAND3

Fig.28



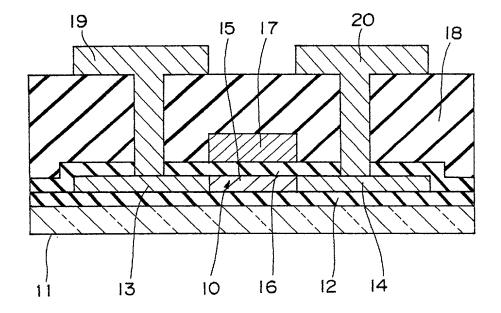


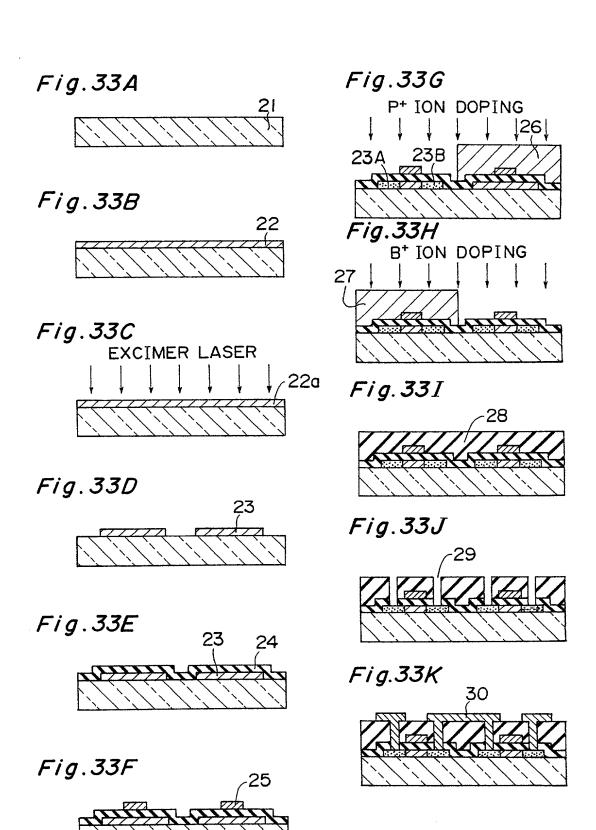


VGEN2 COM VSL VSH SUPPLY VOLTAGE GENERATING CIRCUIT SUB PIX ARY2 |SL1+3 PIX PIX CIRCUIT DATA SIGNAL LINE DRIVE CIRCUIT |SL1+2 \GL VGH PRECHARGE SL1+1 PC2, `GL1+2 SL, **GD2** SD2-SCANNING SIGNAL DRIVE CIRCUIT GL1-GEST GPS PCT PSG SCK SST CT2 CONTROL CIRCUIT

Fig. 31

Fig.32





ÀRY3 PIX PIX SL1+3 CIRCUIT SL1+2 SD3 DATA SIGNAL DRIVE CIRCUI **PC3** PRECHARGE SL-1+1 ار الا Fig. 34 PRIOR ART **GD3** GĽ1+1 SCANNING SIGNAL DRIVE CIRCUIT GL₁ SCK SST GCK GST GEN PCT PSG CONTROL CIRCUIT CT3

SLn

SLn

SW

CL

SW

GL

GL

GL

GL

GL

GL

-ARY4 PIX PIX PIX COM VSL VSH SUPPLY VOLTAGE GENERATING CIRCUIT SUB COM SL 1+3 CIRCUIT SL1+2 VGH VGH 79∧ DATA SIGNAL DRIVE CIRCUI PRECHARGE SL1+1 -GL1+2 SLI FIG. 36 PRIOR ART ·6L1+1 SD47 GD4 SCANNING SIGNAL DRIVE CIRCUIT SCK GCK GST GEN PCT PSG CONTROL CIRCUIT CT4

FLIP-FLOP -S4 FF 7 **NANDS** AS3 FLIP-FLOP -53 FF7 **NAND** /82 AS3 FLIP-FLOP -82 FF7 NAND 5 AS3 121 FLIP-FLOP S FF 7 AS3 SST-SCK -

SL3

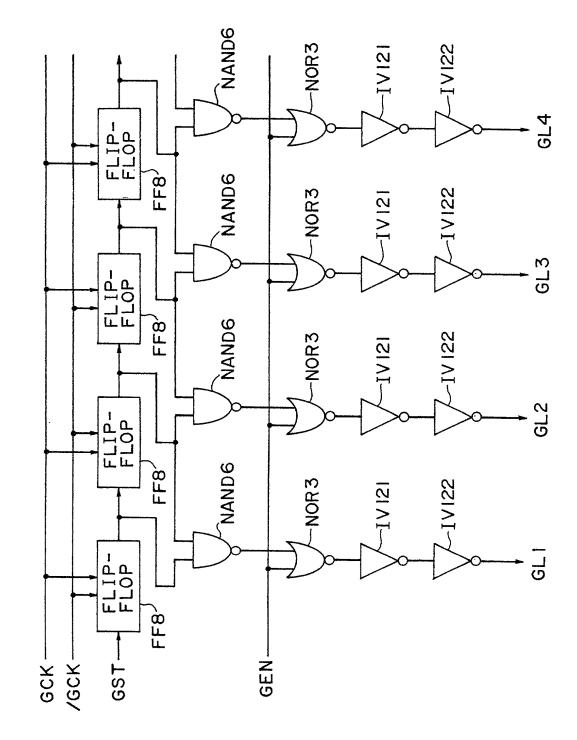
SL2

SL1

NAND

FIG. 37 PRIOR ART

FIG. 38 PRIOR ART



10-TYPE O **TGI41** | TG142 0R D-TYPE O FLIP TG141/ **TGI42** D-TYPE 0 2 ပ **TGI41** TG142 D-TYPE 10 S FLIP-ပ **TGI4I** /CK-있 기 SŢ

TG142

DFF7

DFF7

DFF7

0UT1

DFF7

FIG. 39 PRIOR ART

